PCIE Data Sheet

Features

The features of PCIE include the following:

- Support for all non-optional features and some optional features defined in the *PCI Express Base 3.0* specification.
- Supports 8-bit and 16-bit PHYs through the PIPE
- Ultra-low transmit and receive latency
- Configurable retry buffer size
- Configurable number of outstanding Requests
- Configurable Max_Payload_Size size (128 bytes to 4 KB)
- 4-KB maximum Request size
- Local Address (and Type) Translation Support (Internal and External)
- Very high accessible bandwidth
- 62.5 MHz, 125 MHz, 250 MHz, or 500 MHz operation
- Up to 16 2.5 Gbps or 5.0 Gbps Lanes (x1, x2, x4, x8, or x16)
- Up to 8 8.0 Gbps Gbps Lanes (x1, x2, x4 or x8)
- Automatic Lane reversal as specified in the *PCI Express Base 3.0* specification (transmit and receive)
- Polarity inversion on receive
- Multiple Virtual Channels (VCs)
- Multiple Traffic Classes (TCs)
- Multiple functions
- Supports bypass (Posted and Completion), cut-through, and store-and-forward queues for received TLPs
- Configurable credit management
- Supports ECRC generation and checking
- Supports PCI Express beacon and wake-up mechanism
- Supports PCI Power Management
- Supports PCI Express Active State Power Management (ASPM)
- Supports PCI Express Advanced Error Reporting
- Supports Vital Product Data (VPD)
- Supports PCIe messages for both transmit and receive.
- Configurable filtering rules for Posted, Non-Posted, and Completion traffic
- Configurable BAR filtering, I/O filtering, configuration filtering and Completion lookup/timeout
- Supports two application transmit clients by default, additional third client optional
- Access to configuration space registers and external application memory mapped registers through local bus controller
- Automatic generation of Completions for devices that request RD/WR to application registers through ELBI
- Automatic generation of Completions for Requests that are filtered as Unsupported Request (UR) or Completer Abort (CA) responses

- Supports external priority arbitration (in addition to the internally-implemented transmit arbitration)
- Supports expansion ROM
- Small, low-power option (x1 mode) that reduces the area and has less features
- Implements parity checking on all data buses (optional)
- Implements either parity checking or error checking and correction (ECC) for memories (optional)
- Per-Vector Masking (PVM) in MSI (optional)

Availability

- Q4, 2010

*To obtain more information about the PCIE or other C*Core™ products, please contact the C*Core Technology Co., Ltd. by phone: 0512-68091375, email: support@china-core.com or web: http://www.china-core.com.*

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